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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER

VU, HUNG K

ART UNIT PAPER NUMBER

2811

DATE MAILED: 06/05/2003

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/089,898

Applicant(s)

NAKAMURA ET AL.

Examiner

Hung K. Vu

Art Unit

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 04 December 2002.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-27 is/are pending in the application.
- 4a) Of the above claim(s) 11-27 is/are withdrawn from consideration.
- 5) ☒ Claim(s) 8-10 is/are allowed.
- 6) ☒ Claim(s) 1 and 3-7 is/are rejected.
- 7) ☒ Claim(s) 2 is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on _____ is: a) ☐ approved b) ☐ disapproved by the Examiner.
- If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).
- a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) 2,4,5.
- 4) ☐ Interview Summary (PTO-413) Paper No(s). _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Applicant's election of Invention of Group I, claims 1-10, in Paper No. 8 is acknowledged. Because applicant did not distinctly and specifically point out the supposed errors in the restriction requirement, the election has been treated as an election without traverse (MPEP § 818.03(a)).

Applicant's election without traverse of Invention of Group I, claims 1-10 in Paper No. 8 is acknowledged.

Claims 11-27 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected Invention, there being no allowable generic or linking claim. Election was made **without** traverse in Paper No. 8.

Specification

2. The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

Claim Objections

3. Claims 3 and 8-10 are objected to because of the following informalities:

In claim 3, lines 4-5, and claim 4, line 3-4 "said outer surface portion" should be changed to "said portion of protruding outer surface" for clarity.

In claim 8, line 6, "the bottom" should be changed to "a bottom" for clarity.

In claim 8, line 10, and claim 9, line 2, after "bottom" insert "--surface--" for clarity.

In claim 9, line 2, "the protruding portion" should be changed to "a portion of the protruding conductor" for clarity.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 3-4 are rejected under 35 U.S.C. 102(b) as being anticipated by Youmans (PN 3,761,782).

Youmans disclose, as shown in Figures 10-11, an integrated circuit structure comprising,

a body comprising a semiconductor substrate (11,12) which has a top surface and a bottom surface, wherein one or more through holes (21) pass through the substrate between the top and bottom surfaces, the body comprising one or more circuit elements formed in and/or over the top surface of the semiconductor substrate;

a conductor (41) formed in each through hole and protruding from the bottom surface of the semiconductor substrate, the conductor in each through hole being coupled to one or more of the circuit elements;

a dielectric (18) separating the conductor in each through hole from the semiconductor substrate, wherein at each through hole the dielectric forms a protrusion on the bottom of the body around the conductor;

wherein at each through hole the conductor protrudes from the dielectric on the bottom of the body, the conductor thus having a protruding outer surface not covered by the dielectric, wherein at least a portion of the protruding outer surface is either vertical or sloped outwards (laterally away from the through hole) when the surface is traced down.

With regard to claims 3, Youmans discloses the structure in combination with a first substrate, wherein the protruding outer surface of each conductor is attached to the first substrate with a bonding material (42) to form a conductive bond between the conductor and the first substrate, wherein the bonding material reaches and at least partially covers the outer surface portion which is either vertical or sloped outwards [Figures 10 and 11].

With regard to claims 4, Youmans discloses the bonding material comprises solder which bonds the conductor to the first substrate, wherein the solder reaches and at least partially covers the outer surface portion which is either vertical or sloped outwards [Figures 10 and 11].

5. Claims 1, 3, 4 and 6-7 are rejected under 35 U.S.C. 102(b) as being anticipated by Gnadinger (PN 5,229,647).

Gnadinger discloses, as shown in Figures 4 and 5, an integrated circuit structure comprising,

a body (10) comprising a semiconductor substrate which has a top surface and a bottom surface, wherein one or more through holes (21) pass through the substrate between the top and bottom surfaces, the body comprising one or more circuit elements formed in and/or over the top surface of the semiconductor substrate;

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a conductor (28,20) formed in each through hole and protruding from the bottom surface of the semiconductor substrate, the conductor in each through hole being coupled to one or more of the circuit elements;

a dielectric (24) separating the conductor in each through hole from the semiconductor substrate, wherein at each through hole the dielectric forms a protrusion on the bottom of the body around the conductor;

wherein at each through hole the conductor protrudes from the dielectric on the bottom of the body, the conductor thus having a protruding outer surface not covered by the dielectric, wherein at least a portion of the protruding outer surface is either vertical or sloped outwards (laterally away from the through hole) when the surface is traced down.

With regard to claims 3, Gnadinger discloses the structure in combination with a first substrate (10), wherein the protruding outer surface of each conductor is attached to the first substrate with a bonding material (20) to form a conductive bond between the conductor and the first substrate, wherein the bonding material reaches and at least partially covers the outer surface portion which is either vertical or sloped outwards [Figures 4 and 5].

With regard to claims 4, Gnadinger discloses the bonding material comprises solder which bonds the conductor to the first substrate, wherein the solder reaches and at least partially covers the outer surface portion which either vertical or sloped outwards [Figures 4 and 5].

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With regard to claims 6, Gnadinger discloses the conductor comprises a first conductive layer (20) and a second conductive layer (28) separating the first conductive layer from the dielectric; wherein the second conductive layer is not present on the protruding outer surface [Figure 4].

With regard to claims 7, Gnadinger discloses the first conductive layer is solder wettable, and the second conductive layer is not solder wettable [Col. 3, line 58 – Col. 4, line 36].

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Youmans (PN 3,761,782) in view of Baba et al. (PN 5,969,426).

Youmans discloses all of the claimed limitation as recited in the rejection of claims 1 and 3.

Youmans does not disclose the bonding material fills the entire space between the integrated circuit structure and the first substrate. However, Baba et al. discloses a bonding material (41) fills the entire space between the integrated circuit structure (31) and the first substrate (34).

Note Figures 21d and 22d of Baba et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure of Youmans

having bonding material fills the entire space between the integrated circuit structure and the first substrate, such as taught by Baba et al. in order to provide additionally mechanical support.

7. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Gnadinger (PN 5,229,647) in view of Baba et al. (PN 5,969,426).

Gnadinger discloses all of the claimed limitation as recited in the rejection of claims 1 and 3.

Gnadinger does not disclose the bonding material fills the entire space between the integrated circuit structure and the first substrate. However, Baba et al. discloses a bonding material (41) fills the entire space between the integrated circuit structure (31) and the first substrate (34).

Note Figures 21d and 22d of Baba et al.. Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the structure of Gnadinger having bonding material fills the entire space between the integrated circuit structure and the first substrate, such as taught by Baba et al. in order to provide additionally mechanical support.

Allowable Subject Matter

8. Claim 2 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

9. Claims 8-10 are allowed.

10. The following is an examiner's statement of reasons for allowance:

Applicant's claims 3 and 8-10 are allowable over the references of record because none of these references disclose or can be combined to yield the claimed invention such as throughout each protrusion formed by the dielectric, the dielectric becomes gradually thinner around the adjacent conductor as the protrusion is traced down, as recited in claims 2 and 8.

Conclusion

11. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Hung K. Vu whose telephone number is (703) 308-4079. The examiner can normally be reached on Mon-Thurs 7:00-4:30, alternate Friday 7:00-3:30, Eastern Time.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (703) 308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-7722 for regular communications and (703) 308-7722 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 308-0956.

Vu

May 30, 2003

Hung Vu